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HARMONIC ELIMINATION IN CASCADED MONTICELLO TRANS -Z - SOURCE INVERTER FED INDUCTION MOTOR

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ABSTRACT

Inverters with high-output voltage gain usually face the problem of high-input current flowing through their components. Using high-frequency magnetic devices like transformers or coupled inductors might further worst the problem. Leakage inductances of these devices must strictly be small to prevent overvoltages caused by switching of their winding currents. To avoid these related problems, cascaded trans-Z-source inverters are proposed.Multiple magnetic cells are used in an alternately cascading pattern rather than a single magnetic cell with large turns ratio. Simulation and experimental results have shown that the multicell inverters can produce the same high-voltage gain, while keeping currents and voltages of the components low. The inverters can also step down their output voltages like a traditional voltage-source inverter and the THD contents in output voltage of inverters can also be significantly reduced.

Index Terms—Cascaded inverters, coupled inductors, highfrequency magnetic, transformers, Z-source inverters.

1. INTRODUCTION

Traditionalvoltage-source inverters(VSIs)alone are, therefore, not satisfactory since they only step down voltages. To introduce an additional boost functionality, dc–dc boost converters can be placed before the VSIs or current-source inverters (CSIs) can be used instead. Both inverters have some amount of boost inductance added to their dc circuits, which certainly is a common modification introducedto inverters with boost functionality (if switched-capacitor technique is not used). The inductance added to a CSI is usually larger to keep its dc input current constant. This, together with other disadvantages like tougher control and lack of standard semiconductor modules for implementation, usually limits the use of CSIs, as compared to VSIs. Other topologies for consideration include those single-stage buck–boost inverters designed with either voltage-source (VS) or current-source (CS) characteristics. One example can be found in [1], where a Cuk or single-ended primary-inductor converter dc–dc converter is placed in front of the traditional VSI. Instead of operating them independently, their commutations are coordinated to form an eventual single-stage entity after removing redundant semiconductor and passive components. The same approach can be applied to other dc–dc converters, resulting in other single-stage circuits being proposed [2]. Among the noticeable is the Z-source inverters proposed in [3]. Being slightly different, the Z-source dc–ac inverter was proposed before various Z-source dc–dc converters surfaced. Despite that, it is still appropriate to represent a Z-source inverter as a combination of Z-source dc–dc converter and an inverter after removing redundant semiconductor and passive components. Both VS- and CS-type Z-source inverters have been developed. But, as per traditional inverters, interest in the former is presently more intensive with its modulation, dynamics, control, and sizing studied in [4]–[7], respectively. Related applications have also been tried like in motor drives [8], solar generation, [9], and electric vehicles [10]. These references used the same basic Z-source impedance network. Changes to the basic network were eventually made in [11]–[14] with the modified networks named as improved, quasi, and embedded Z-source networks. Although named differently, these networks are mostly similar.Subsequently merged the variations. The outcome was a generic network each for VS-type and CS-type Z-source inverters. It was also clarified in [15] that the main differences among the existing networks are their different source placements, which surprisingly give them their unique advantages. Other features like the number of *LC* components and input-to-output gain remain unchanged. The latter was subsequently raised as a concern in [15] and [16], where additional inductors, capacitors, and diodes were used to raise the voltage gain of a VS-type Z-source inverter.

This might be helpful for renewable energy generation, where low-source voltages need to be boosted to higher common ac voltage for grid interfacing. However, the amount of components added might not be economically justifiable, even though it was an understandable beginning for obtaining high-voltage gain. In [17]–[20], the authors subsequently demonstrated the use of coupled inductors transformers for raising their voltage gains. Although [17] gives a slightly higher gain than the others, it uses more coupled inductors and diodes. It also has no reduction in the number of capacitors. It is thus not discussed further. On the contrary, the circuits presented in [19] and [20] use only one coupled transformer with two windings and a finite magnetizing inductance like in a flyback dc–dc converter. They also use one lesser capacitor than the basic Z-source network. Because of this, the networks no longer have an X-shape.

2. TRANS-Z-SOURCE INVERTERS

A review of trans-Z-source inverters is presented here to recap on some basis operating principles, before identifying a few shortcomings. Based on this understanding, the CMC trans-Z source inverters are proposed in the following section.

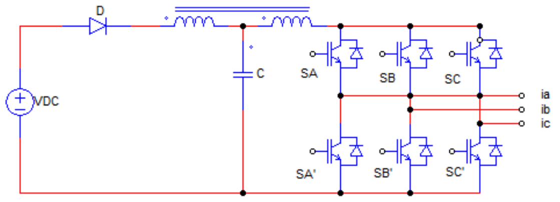

Fig.1(a).Trans-z-source inverter with source placed in series with diode D

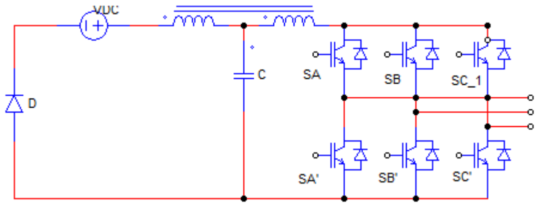

Fig.1(b).Trans-z-source inverter with source placed in series with VSI bridge

A. Operating Principles

Fig. 1 shows two VS-type trans-Z-source inverters, whose operating principles are closely similar. Because of that, only Fig. 1(a) is considered with its operating states shown in Fig. 2. In the shoot-through state, the trans-Z-source inverter has two of its switches from the same phase leg turned ON to imitate the boost switch found in a classical dc–dc boost converter [e.g., SA and SA'in Fig. 1(a)]. Simultaneously, input diode*D* reverse biases to form an open circuit. Voltages $VW\ 1$ and $VW\ 2$ across the coupled windings *W*1 and *W*2 can then be written as

$$VW\,1 = VC, VW\,2 = \gamma 2 VW\,1\ . \qquad (1)$$

where*VC* represents voltage across the capacitor, and *γ*2 represents turns ratio of *W*2 to *W*1. Upon removing the short circuit, a nonshoot-through state is formed, whose equivalent circuit is shown in Fig. 2(b). Unlike Fig. 2(a), the right of Fig. 2(b) is replaced by a current source for representing the VSI bridge and external ac load. The value of this current source can either be nonzero when in a traditional VSI active state or zero when in a null state. In total, there are six active and two null states. Also shown in Fig. 2(b), the conduction of input diode *D* can firmly connect the input source *V*dc to the rest of the circuit. Based on this representation, voltages $VW\ 1$ and $VW\ 2$ can be written as

$$VW\,1 = VW\,2/\gamma 2\ ; VW\,2 = V\mathrm{dc} - VC\ .(2)$$

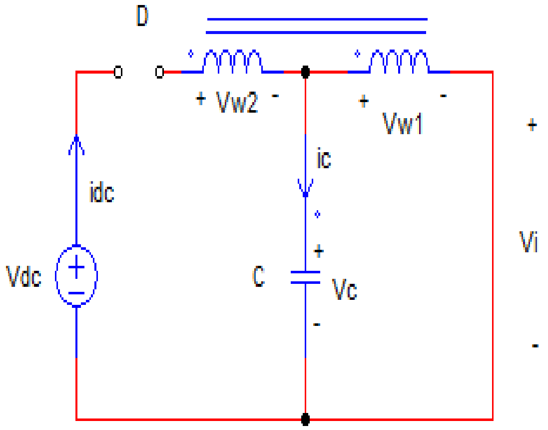

Fig .2(a). Equivalent circuits of Fig.1 when in shoot-through state

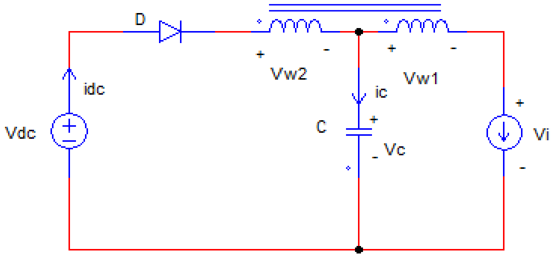

Fig 2(b).Equivalent circuits of Fig.1 when in nonshoot-through states.

Since winding voltages per switching period will average to zero, (1) and (2) can be combined as

$$dST VC + (1 - dST)(Vdc - VC)/\gamma 2 = 0 \quad (3)$$

where$dST$is the fractional time during which the inverter is in its shoot-through state. This time is usually kept constant to avoid introducing low-order ripple to the inverter voltages and currents. Simplifying then leads to

$$VC = Vdc(1 - dST)/(1 - (\gamma 2 + 1)dST). \quad (4)$$

In the nonshoot-through state, the dc-link voltage applied tothe load when in an active state is written as

$$V'i = VC - vW1 .$$

Upon substituted by (2) and (4), $v'i$becomes

$$V'i = Vdc/(1 - (\gamma 2 + 1)dST) . \quad (5)$$

When modulated appropriately, this dc-link voltage gives riseto the following peak ac amplitude $v'ac$as

$$V'ac = Mv'i/2 = 0.5\ MVdc/(1 - (\gamma 2 + 1)dST)(6)$$

Where$M$ (≤ 1.15 with triple offset introduced) represents theinverter modulation index. The denominator of (6) must clearlybe greater than zero, and as understood from [3] and [4], theshoot-through state can only replace the traditional null state.Because of these two restrictions, $dST$and M are constrainedby the following inequalities:

$$dST < 1/(\gamma 2 + 1); \ M \leq 1.15(1 - dST) . \ (7)$$

Assuming that$M = 1.15(1 - dST)$ for producing the greatestvoltage boost, (6).

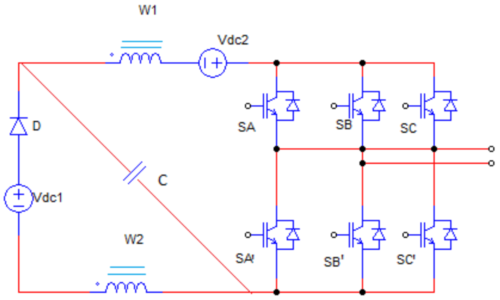

Fig.3.Trans-z-source cell

The demanded voltage gain can clearly be raisedby increasing dST or $\gamma 2$. The former means lowering$M$, whichgenerally is not preferred since it leads to poor dc-link utilizationand hence unnecessarily high-voltage stresses across thecomponents. Increasing $\gamma 2$ is therefore a better alternative if thetransformer can be designed accordingly, while yet maintainingexcellent coupling.The same averaging process can be applied to the secondtrans-Z-source circuit drawn in Fig. 1(b) with the same voltageexpressions in (5) and (6) produced. Its different sourceplacement mainly leads to a lower capacitor voltage written as

$$VC = Vdc\gamma 2dST/(1 - (\gamma 2 + 1)dST).(8)$$

Since its source is in series with the lower voltage winding $W1$, the circuit in Fig. 1(b) unfortunately experiences a higher instantaneous source current. Flow of such high current can either damage the source or demand for a larger low-pass filter, which certainly is undesirable.

3. CMC TRANS-Z-SOURCE INVERTERS

To avoid direct series connection, an alternate cascading technique is discussed after describing the generic trans-Z-source cell shown in Fig. 5. Unlike Fig. 1, the generic cell in Fig. 5 has two dc sources labeled as V 'dc and V "dc. When they are set as V 'dc = $Vdc$and V"dc = 0, the network in Fig. 1(a) is obtained.Inversely, for $V'dc = 0$and $V''dc = Vdc$, the network in Fig. 1(b) is produced. Fig. 5 is, therefore, a generic representation of the two networks shown in Fig. 1. Moreover, it is intentionally drawn with an X-shaped structure that resembles the original Z-source network proposed in [3]. With this X-shaped cell, the alternate cascading technique can be performed based on the following few steps:

1) Begin with cell 1 with its windings labeled as $W11$ and $W2$;

2) Duplicate a copy of cell 1, and name it as cell2.Windings of cell 2 are labeled as$W12$ and$W3$ with their turns ratio marked as $\gamma 3$;

3) Flip cell 2 vertically and place it below cell 1;

4) Merge cell 1 and cell 2 with $W2$ of cell 1 replacing $W12$ of cell 2;

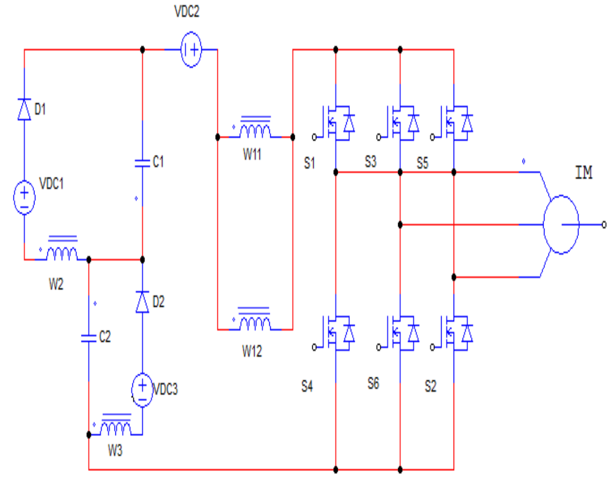

Fig.4.proposed CMC trans-z-source inverter

5) Shift $W12$ of cell 2 to be in parallel with $W11$ of cell1;

6) Duplicate cell k with windings $W1k$ and $W(k + 1)$, and turns ratio γk+1;

7) Repeat the flipping and merging until all N cells are cascaded (until $k = N$).

The proposed CMCtrans-Z-source inverter is shown in Fig.3, which clearly does not have any direct series connection. No balancing resistors and losses are therefore needed, meaning that the inverter in Fig.3 is likely more efficient than the direct series-connected circuit. The CMC inverterwould however still require parallel connections of windings $W1k$ ($k = 1$ to N) and capacitors to manage the flow of high instantaneous current during shoot through. Such parallel connections will not be a concern in practice, unlike series connections.Beginning with the shoot-throughstate with the VSI bridge shorted and all diodes reverse biased. Their correspondences when in the nonshoot-through stateall diodes are conducting.

A generic representation of the CMC trans-Z-source inverter with all possible source locations shown in Fig.4.These sources can be set to zero, where desired, with only one of them needed to be nonzero for powering the inverter. can however be realized usinglower rated components that might be more readily available orfit the layout of an application better.

Unlike those uncontrollabledistributions of voltages, the circuit in Fig.3 also realizes more deterministic distributions of voltages across the diodes and capacitors. Such distributions have no dependence on the component internal parameters. Instead, they depend solely on the chosen divisions of transformerturns ratio γk+1 and source voltage, which can freely be decided by the designer, depending on the scenario under consideration. (At least a larger capacitance can now be made to share a higher voltage stress unlike in direct series connection).

Thepresented cascaded trans-Z-source inverter is thus an alternative topology for considerationwith both high-gain stresses and low component stresses. Its prospective applications can be in the area of connecting green sources like fuel cells, photovoltaicsources, and other low-voltage dc sources to the mains or local microgrids. Related control techniques for these applications will be left for a future investigation since the topic of concern here is more on topological development.

4. SIMULATION RESULTS

In order to verify the validity of the topology the intended inverter is fed with an induction motor. A complete mathematical model of the CMC inverter is developed and simulated using MATLAB / SIMULINK to investigate the performance of the inverter. From the simulation it is verified THD is comparably reduced to that of conventional system.

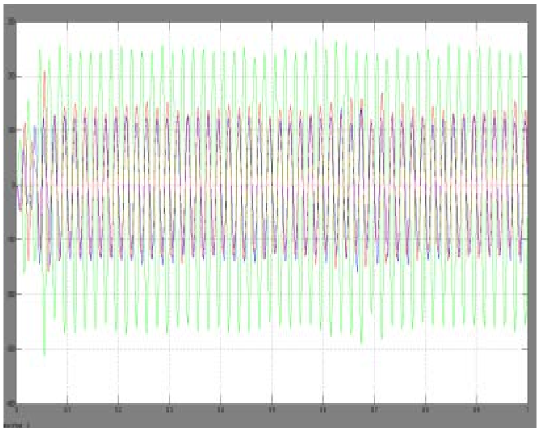

Fig.6.Three phase output voltage waveform of CMC inverter

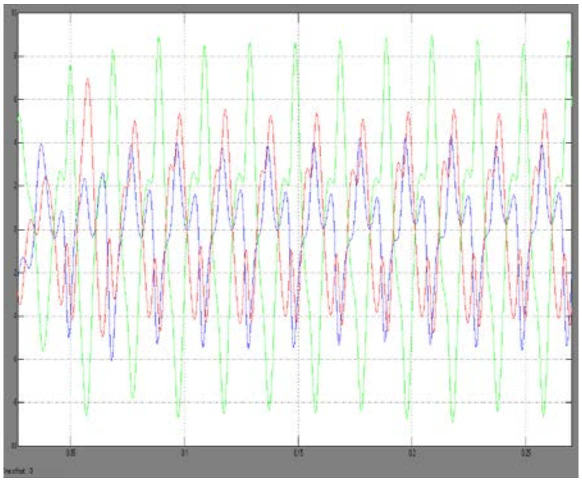

Fig.7.Three phase output current waveform of CMC inverter

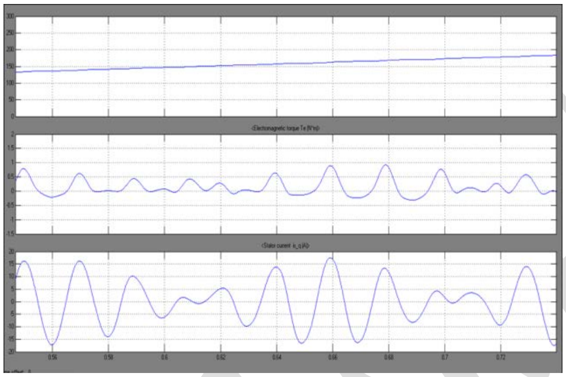

Fig.8. stator current, rotor speed, electromagnetic torque, dc bus voltage waveform

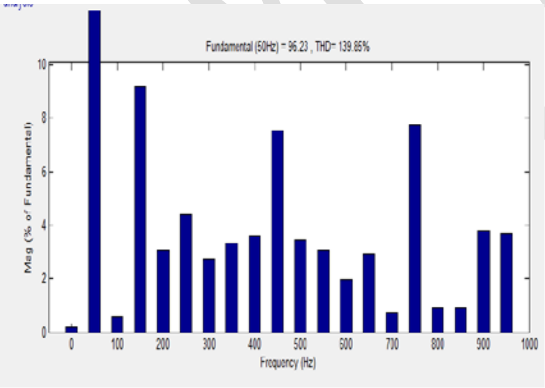

Fig.9. THD output waveform for existing system

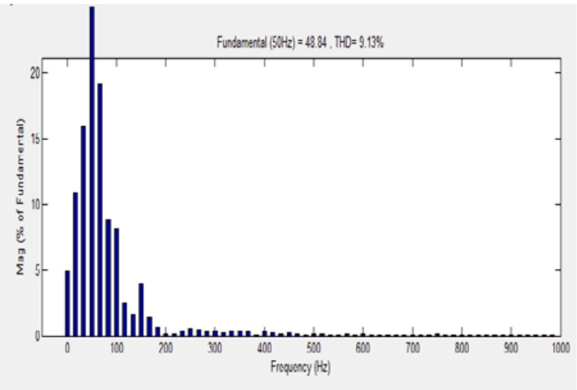

Fig.9.THD output waveform for proposed system

5. CONCLUSION

In this paper a generic trans-Z-source cell is presented, which can be duplicated and alternately cascaded to form various CMC trans-Z-source inverters with different source placements. Although the inverters use multiple components to tolerate higher voltage gains, they do not rely on direct series connections of the components. Common voltage sharing problems that vary randomly with parameters are therefore not experienced by the proposed CMC trans-Z-source inverters. Moreover, by using smaller coupled transformers with lower turns ratios, the proposed inverters divide their instantaneous current stresses among windings better. The main advantage of CMC inverter topology is it reduces THD in the output voltage increased efficiency.

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